

The figure contains two schematic diagrams, (a) and (b), showing a cross-section of a photocopier drum assembly. Both diagrams show a drum core (11) with a conductive layer (12) and a photoconductive layer (14) on top. The photoconductive layer (14) is divided into a central region (131) and two side regions (132). The side regions (132) are connected to a negative terminal (-) and the central region (131) is connected to a positive terminal (+). In diagram (a), the central region (131) is positively charged (indicated by '+' signs) and the side regions (132) are negatively charged (indicated by '-' signs). An arrow labeled 'LIGHT' points upwards from the central region (131). In diagram (b), the central region (131) is negatively charged (indicated by '-' signs) and the side regions (132) are positively charged (indicated by '+' signs). An arrow labeled 'LIGHT' points upwards from the central region (131). The drum core (11) is connected to a positive terminal (+) in (a) and a negative terminal (-) in (b).

A cross-sectional view of a semiconductor device. It shows a substrate 21 with a thin layer 22 on top. Two electrodes, 23 and 25, are formed on the surface. Electrode 23 is connected to a positive terminal (+) and electrode 25 to a negative terminal (-). A layer 24 is formed over the electrodes and substrate. A layer 26 is formed on top of layer 24. The device is shown in a cross-sectional view with various layers and electrodes labeled with numbers and signs.

Figure 1 consists of six cross-sectional views of a semiconductor device, labeled (a) through (f), illustrating the sequential steps of its fabrication:

- (a)** Shows a substrate (21) with a first conductive layer (22) formed on its top surface.
- (b)** Shows the formation of a second conductive layer (271) on top of the first conductive layer (22). The second conductive layer (271) is patterned to form a raised portion (281).
- (c)** Shows the formation of a third conductive layer (23) on top of the second conductive layer (271). The third conductive layer (23) is patterned to form a raised portion (24).
- (d)** Shows the formation of a fourth conductive layer (272) on top of the third conductive layer (23). The fourth conductive layer (272) is patterned to form a raised portion (282).
- (e)** Shows the formation of a fifth conductive layer (25) on top of the fourth conductive layer (272). The fifth conductive layer (25) is patterned to form a raised portion (26).
- (f)** Shows the final device structure with the fifth conductive layer (25) and its raised portion (26) on top of the fourth conductive layer (272) and its raised portion (282).

Fig. 4

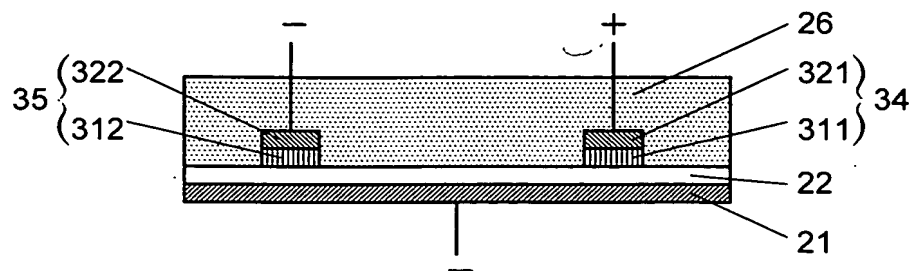


Fig. 5

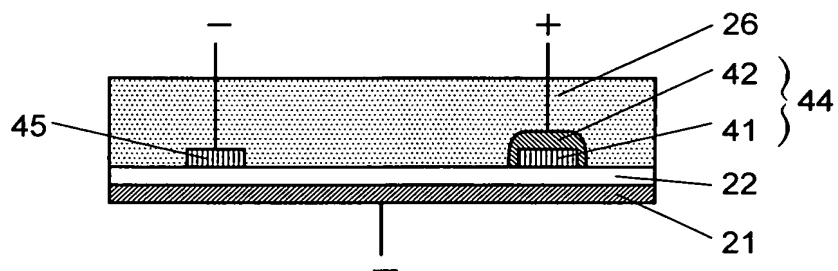


Fig. 6

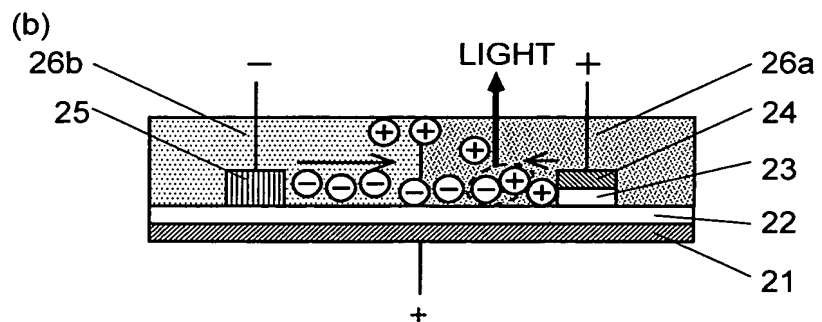
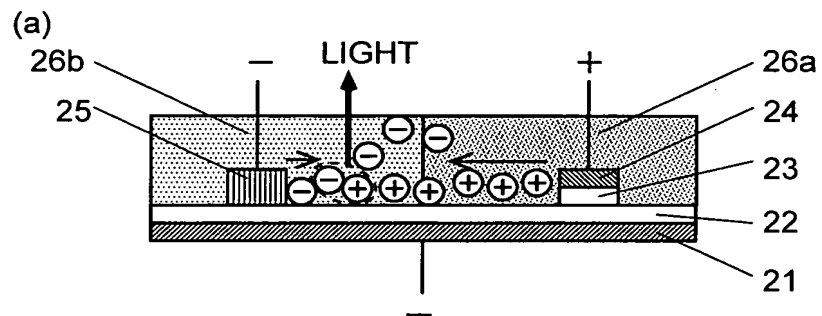


Fig. 7

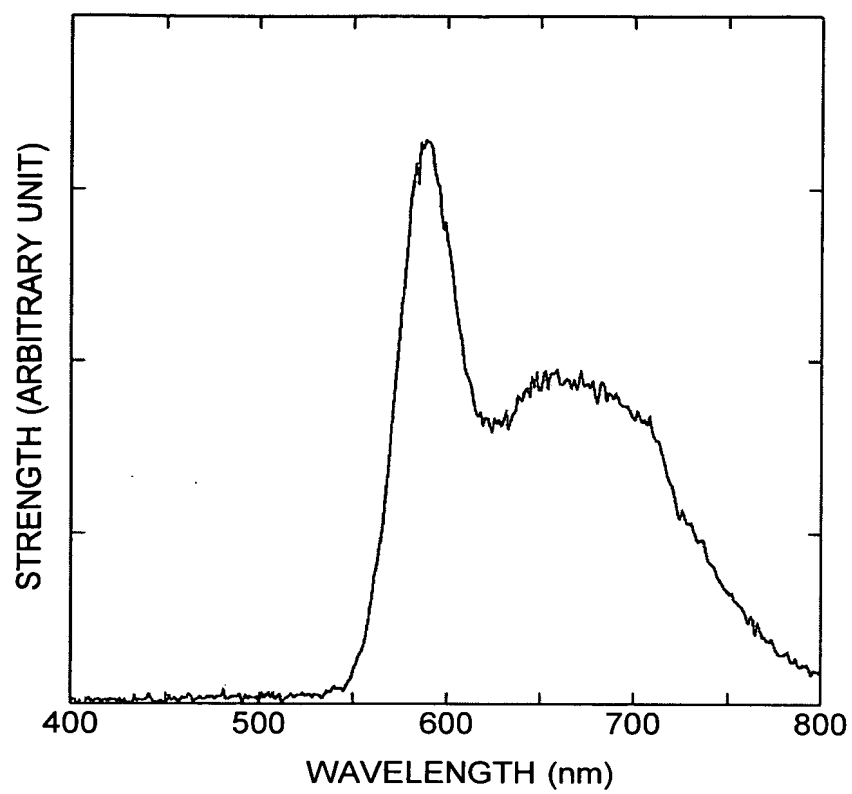


Fig. 8

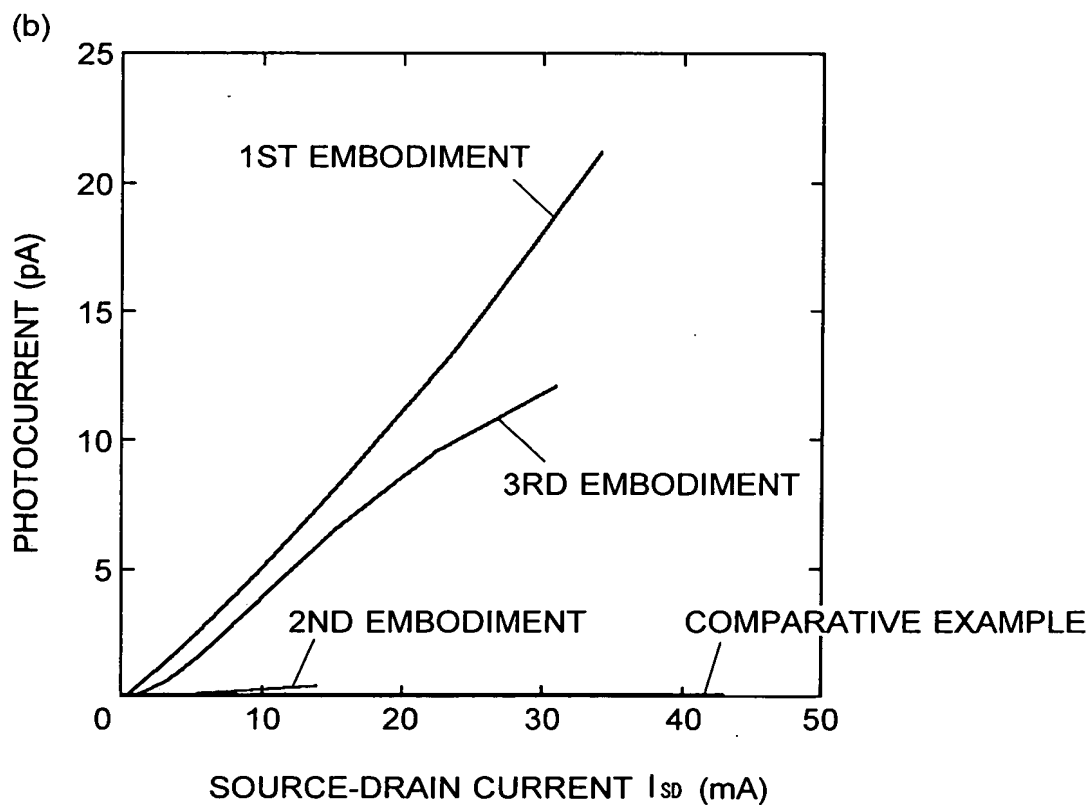
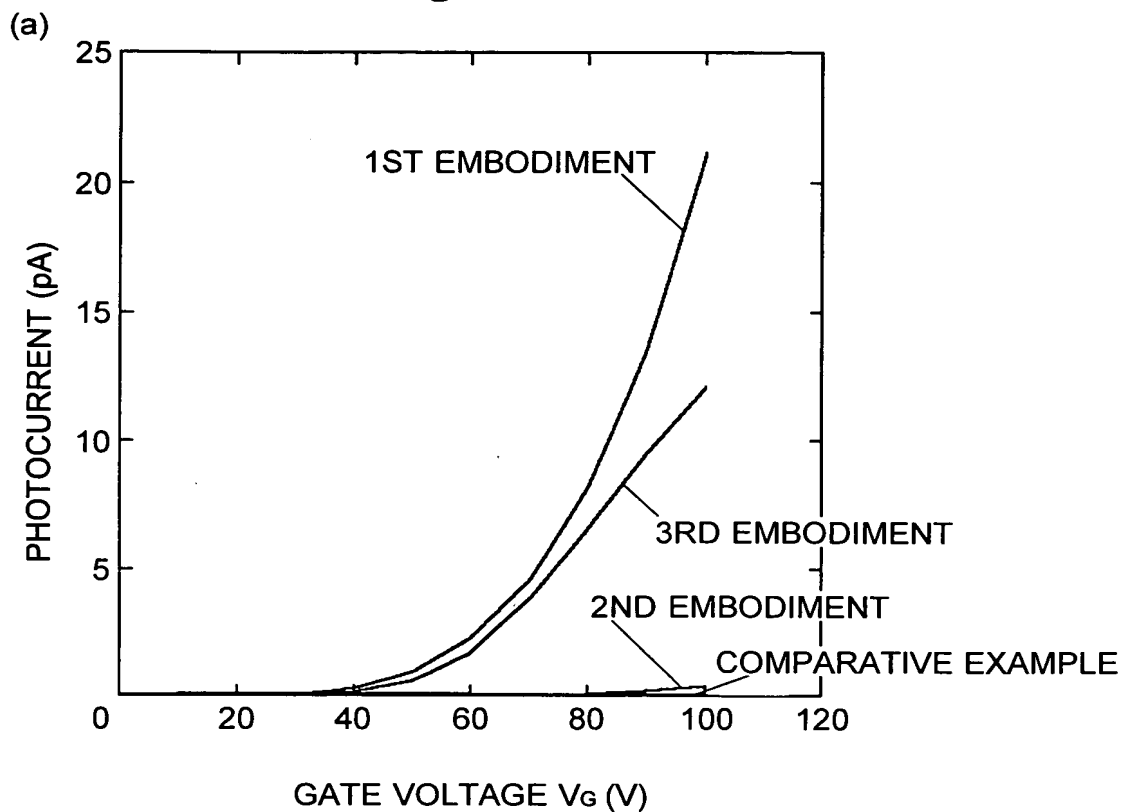


Fig. 9

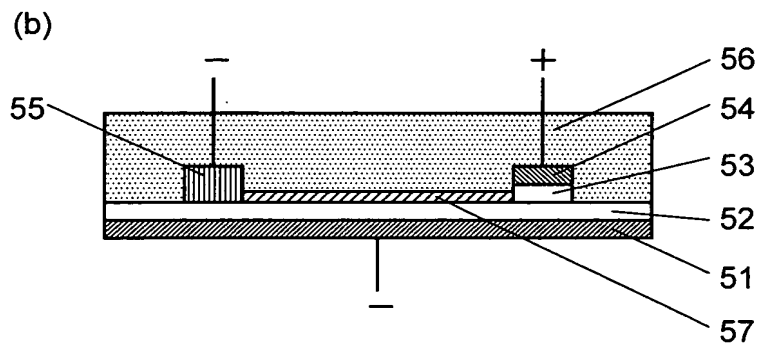
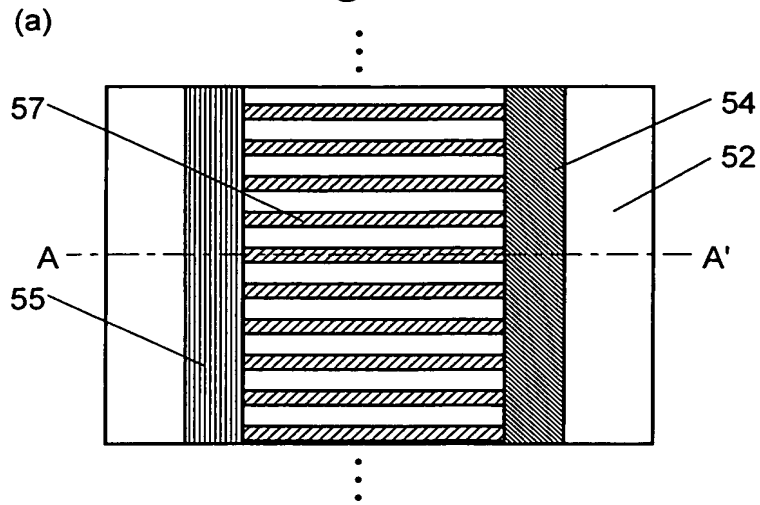


Fig. 10

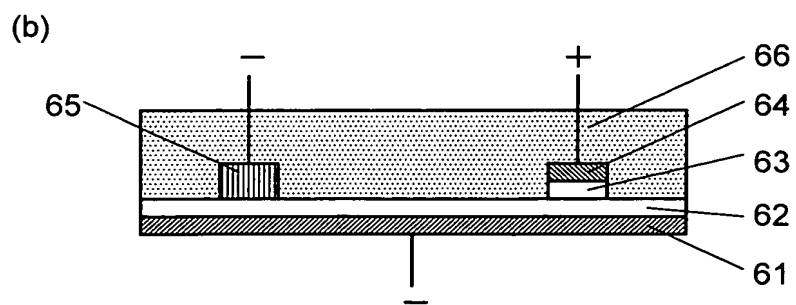
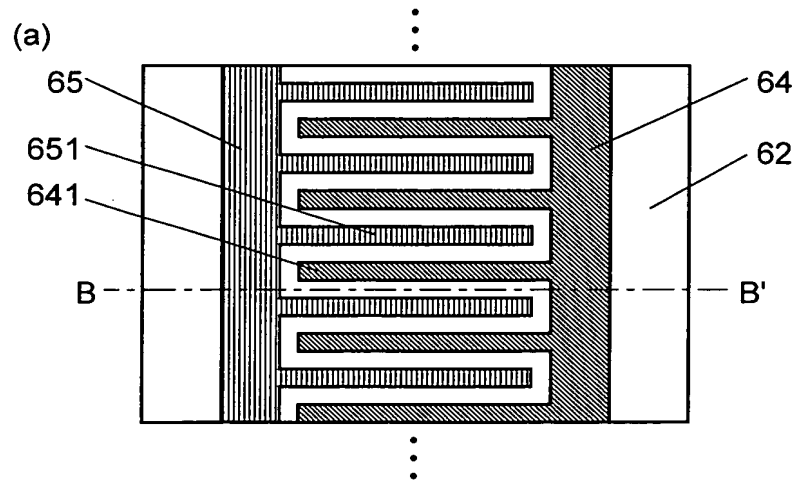


Fig. 11

